Docket No.: SON-2903
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Noboru Toyozawa et al.

Application No.: 10/541,092 | Confirmation No.: 4260

Filed: June 29, 2005 | Art Unit: 2629

For: DISPLAY DEVICE | Examiner: Yuk Chow

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated January 28, 2009. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately. This brief is in furtherance of the Final Office Action of January 28, 2009.

A Notice of Appeal was filed in this case on April 22, 2009, along with a Request for Panel Review. The Notice of Panel Decision from Pre-Appeal Brief Review dated June 22, 2009 ("the Decision) indicates that claims 17-26 remain rejected.

The Decision further indicates that the extendable time period for the filing of the Appellant's Brief will be reset to be one month from the mailing of the Decision. Accordingly, the filing of this Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 017243, frame 0014.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Within the Final Office Action of January 28, 2009:

Paragraph 2 indicates a rejection of claims 17, 18 and 23-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,567,066 (Hashimoto).

Paragraph 4 indicates a rejection of claims 19-22 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).

Paragraph 5 indicates a rejection of claim 26 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).

Thus, the status of the claims is as follows:

Canceled: Claims 1-16

Rejected: Claims 17-26

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 17-26 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Provided is a statement of the status of any amendment filed subsequent to final rejection.

Subsequent to the final rejection of January 28, 2009, no amendment has been filed in this case.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following description is provided for illustrative purposes and is not intended to limit the scope of the invention. Reference is made to the Substitute specification filed on February 15, 2006.

17. A display device comprising:	
a matrix of pixels, a pixel of said matrix of pixels having an electro-optic material between a pixel electrode and a common electrode;	Paragraph beginning at page 10, line 23
a common driver having an offset circuit, a common voltage generated by said common driver being applied to said common electrode,	Paragraph beginning at page 10, line 23
wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.	Paragraph beginning at page 13, line 24

18. The display device as claimed in claim 17, wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage.	Paragraph beginning at page 20, line 19

19. The display device as claimed in claim 18, wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.	Paragraph beginning at page 20, line 5

20. The display device as claimed in claim 19, wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.	Paragraph beginning at page 20, line 5

21. The display device as claimed in claim 18, wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.	Paragraph beginning at page 13, line 24

22. The display device as claimed in claim 21, wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.	Paragraph beginning at page 16, line 16

26. An electronic device capable of switching between a normal power consumption state and a low power consumption state, the electronic device comprising:	
the display device as claimed in claim 17, the matrix of pixels being within a display area; and	Paragraph beginning at page 10, line 23
a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode;	Paragraph beginning at page 17, line 2
wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.	Paragraph beginning at page 17, line 2

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

- Whether the Examiner erred in rejecting claims 17, 18 and 23-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,567,066 (Hashimoto).

- Whether the Examiner erred in rejecting claims 19-22 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).

- Whether the Examiner erred in rejecting claim 26 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).

These issues will be discussed hereinbelow.

VII. ARGUMENT

In the Final Office Action of January 28, 2009:

> The Examiner erred in rejecting claims 17, 18 and 23-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,567,066 (Hashimoto).
>
> The Examiner erred in rejecting claims 19-22 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).
>
> The Examiner erred in rejecting claim 26 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

1. **The Examiner erred in rejecting claims 17, 18 and 23-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,567,066 (Hashimoto).**

Claims 17 and 23-25 - Claims 23-25 are dependent upon claim 17. Claim 17 is drawn to a display device comprising:

> a matrix of pixels, a pixel of said matrix of pixels having an electro-optic material between a pixel electrode and a common electrode;
>
> a common driver having an offset circuit, a common voltage generated by said common driver being applied to said common electrode,
>
> wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.

Hashimoto - Hashimoto arguably discloses gray shade voltages VX0-VX9 (Hashimoto at Figures 1, 2, 9, 10).

However, Hashimoto ***fails*** to disclose, teach, or suggest that the output offset control circuit 14 is charged to an offset voltage at a time of a rising edge of any of the gray shade voltages VX0-VX9.

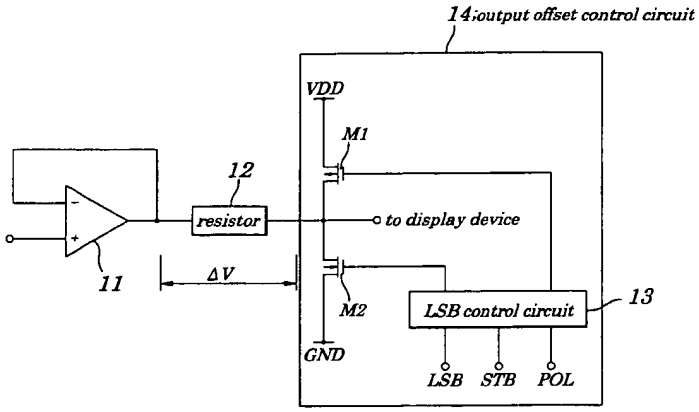
Hashimoto arguably discloses supply voltage VDD (Hashimoto at Figure 5).

However, Hashimoto ***fails*** to disclose, teach, or suggest that the output offset control circuit 14 is charged to an offset voltage at a time of a rising edge of supply voltage VDD.

Instead, the Office Action contends that Hashimoto discloses a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage (Fig. 5, M1 which is connected to VDD and Fig. 6, offset circuit is charged when M1 is on), said offset voltage adjusting a level of said common voltage (Fig. 6(ΔV)) (Office Action at page 2).

In response, Figure 5 of Hashimoto is provided hereinbelow.

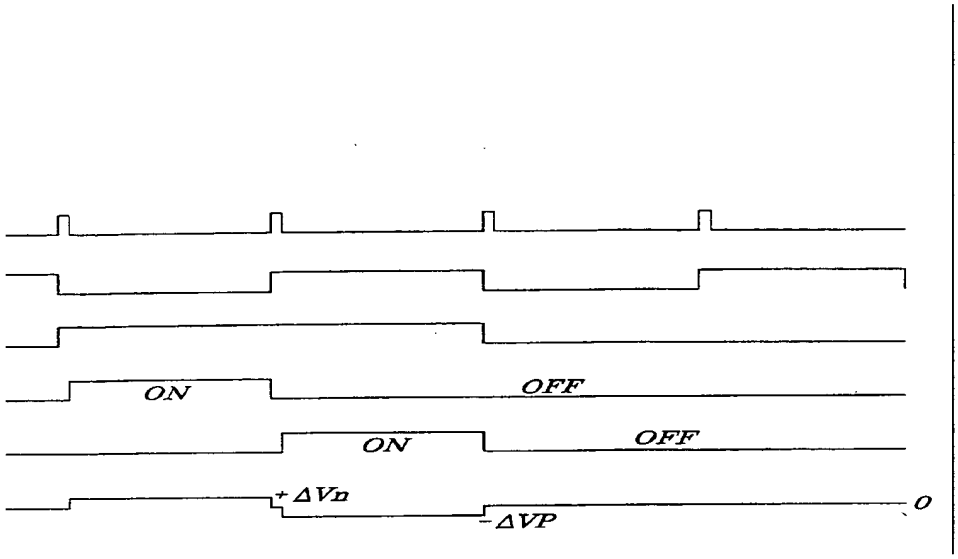
FIG.5



Hashimoto arguably discloses at column 7, lines 7-23, that:

> FIG. 5 is a schematic block diagram showing first and second output circuits shown in FIG. 1. Each of the output circuits is provided with an operational amplifier 11 used to amplify an output signal fed from the gray shade voltage selecting circuit and to convert its impedance. Between the operational amplifier 11 and an output terminal connected to the display device is connected a resistor 12 including an analog switch or the like. Between the resistor 12 and the output terminal are connected transistors M1 and M2 drains of which are connected to each other. A source of the transistor M1 is connected to a terminal of supply voltage VDD and a source of the transistor M2 is connected to a ground GND. Gates of the transistors M1 and M2 are connected to an LSB control circuit 13. To the LSB control circuit 13 are inputted the least significant bit (1 bit) of the digital image data and polarity signal POL and latch signal STB. That is, *an output offset control circuit 14 is composed of transistors M1 and M2 and of the LSB control circuit 13*.

Furthermore, Figure 6 of Hashimoto is provided hereinbelow.



The paragraph of Hashimoto beginning at column 8, line 13, arguably discloses that:

> FIG. 6 is a time chart showing operations of the first output circuit 9 according to the first embodiment. In the first output circuit 9, if the least significant bit LSB is 0 (low), both of the transistors M1 and M2 are turned OFF regardless of the polarity signal POL. At this point, the voltage drop in the resistor 12 including analog switches or the like does not occur because currents do not flow constantly, an output voltage supplied from the operational amplifier 11, as it is, is applied to the display device from the output terminal.

The paragraph of Hashimoto beginning at column 8, line 22, arguably discloses that:

> On the other hand, if the least significant bit LSB is 1 (high), by the polarity signal POL, either of the transistor M1 or M2 is turned ON. That is, if the polarity signal POL is 0 (low), a negative polarity voltage from the second gray shade selecting circuit 8 is applied to the operational amplifier 11 of the first output circuit 9, the transistor M1 is turned ON and the transistor M2 remains OFF. Therefore, a steady

state current Im1 flows through the transistor M1 and, since the supply voltage VDD is supplied to a source of the transistor M1, a voltage rise of $\Delta Vn=Im1\times Rm$ occurs at the resistor 12.

Here, the transistors M1 and M2 of Hashimoto are switched ON or OFF by the LSB control circuit 13 ***based on the least significant bit of the digital image data*** (Hashimoto at column 7, lines 29-31).

In this regard, the Office Action ***fails*** to show that *the least significant bit of the digital image data* of Hashimoto and a *power supply voltage* are one in the same, especially when Figure 5 of Hashimoto appears to depict the least significant bit LSB as being something other than supply voltage VDD.

Likewise, Figure 6 of Hashimoto ***fails*** to show the switching of either transistor M1 or transistor M2 on a rising edge of any signal.

- ***Thus, Hashimoto fails to disclose, teach, or suggest a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Claim 18 - Claim 18 is drawn to the display device as claimed in claim 17, wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

Hashimoto arguably discloses that a source of the transistor M1 is connected to a terminal of **supply voltage VDD** and a source of the transistor M2 is connected to a ground GND. Gates of the transistors M1 and M2 are connected to an LSB control circuit 13 (Hashimoto at column 7, lines 16-19).

Hashimoto arguably discloses that therefore, a steady state current Im1 flows through the transistor M1 and, since the **supply voltage VDD** is supplied to a source of the transistor M1, a voltage rise of $\Delta Vn=Im1\times Rm$ occurs ***at the resistor 12*** (Hashimoto at column 8, lines 28-33).

Hashimoto arguably discloses that therefore, since the steady state current Im2 flows through the transistor M2 and the source of the transistor M2 is connected to a ground GND, a voltage drop of $\Delta Vp=Im2\times Rm$ occurs ***at the resistor 12*** (Hashimoto at column 8, lines 39-42).

Nevertheless, the Office Action fails to show the presence within Hashimoto of a ***falling edge of the supply voltage VDD***.

As a consequence, Hashimoto ***fails*** to disclose, teach, or suggest that an offset circuit is discharged at a time of a ***falling edge of the supply voltage VDD***.

- ***Thus, Hashimoto fails to disclose, teach, or suggest a device wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage.***

2. **The Examiner erred in rejecting claims 19-22 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).**

Claim 19 - Claim 19 is drawn to the display device as claimed in claim 18, wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

In addition, Hashimoto is ***silent*** as to the presence of an insulating substrate.

- ***Thus, Hashimoto <u>fails</u> to disclose, teach, or suggest a device wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.***

<u>Maekawa</u> - The Office Action cites Maekawa for the features that are deficient from within Hashimoto.

However, the Office Action ***<u>fails</u>*** to show within Maekawa the presence of a rising edge of a power supply voltage VCC.

- ***Thus, the Office Action <u>fails</u> to show that Maekawa discloses a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Additionally, the paragraph of Maekawa beginning at column 4, line 38, arguably discloses that:

> FIG. 4 is a schematic view showing an example of a configuration of a liquid crystal display device to which the present invention is applied. In FIG. 4, a liquid crystal panel 22 is constructed by arranging liquid crystal cells (pixels) 21 two-dimensionally in a matrix shape, with a vertical (row) driver 23 for carrying out row selections and a horizontal (column) driver for carrying out column selections being provided at the periphery of the liquid crystal panel 22. The liquid crystal panel 22 and peripheral circuits thereof, namely the vertical driver 23 and the horizontal driver 24, are integrally formed of polysilicon.

However, the Office Action ***<u>fails</u>*** to show within Maekawa the presence of an insulating substrate.

- ***Thus, the Office Action <u>fails</u> to show that Maekawa discloses a device wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.***

Claim 20 - Claim 20 is drawn to the display device as claimed in claim 19, wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

In addition, Hashimoto is ***silent*** as to the presence of an insulating substrate.

- ***Thus, Hashimoto fails to disclose, teach, or suggest a device wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.***

Maekawa - As noted hereinabove, the Office Action ***fails*** to show within Maekawa the presence of an insulating substrate.

- ***Thus, the Office Action fails to show that Maekawa discloses a device wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.***

Claim 21 - Claim 21 is drawn to the display device as claimed in claim 18, wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

In addition, Hashimoto is ***silent*** as to the presence of a coupling capacitor within said offset circuit.

- ***Thus, Hashimoto fails to disclose, teach, or suggest a device wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.***

Maekawa - The paragraph of Maekawa beginning at column 3, line 47, arguably discloses that:

> First, in a precharge period T1, the first and second analog switches 15 and 16 are turned on and the third analog switch 17 is turned off. As a result, a specific precharge voltage Vpre is applied to the gate of the source follower transistor 11 from the precharge supply 14 via the first analog switch 15. At this time, ***a charge*** *corresponding to an amount of* ***offset*** *Vos (=Vgs) is accumulated at the* ***capacitor 13*** connected across the gate and source of the source follower transistor 11.

Recall, *claim 17 of the instant application includes that* said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, *said offset voltage adjusting a level of said common voltage*.

Within claim 21, said common driver has a start circuit, said start circuit *charging a coupling capacitor within said offset circuit to said offset voltage*.

As noted hereinabove, the Office Action ***fails*** to show the ***offset*** *Vos* of Maekawa as "*adjusting a level of said common voltage*". In this regard, the Office Action ***fails*** to show the "*offset Vos*" of Maekawa and the "*offset voltage*" of claim 21 as being one in the same.

- ***Thus, the Office Action fails to show that Maekawa discloses a device wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.***

Claim 22 - Claim 22 is drawn to the display device as claimed in claim 21, wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

Hashimoto arguably discloses that a source of the transistor M1 is connected to a terminal of **supply voltage VDD** and a source of the transistor M2 is connected to a ground GND. Gates of the transistors M1 and M2 are connected to an LSB control circuit 13 (Hashimoto at column 7, lines 16-19).

Hashimoto arguably discloses that therefore, a steady state current Im1 flows through the transistor M1 and, since the **supply voltage VDD** is supplied to a source of the transistor M1, a voltage rise of $\Delta Vn=Im1\times Rm$ occurs at the resistor 12 (Hashimoto at column 8, lines 28-33).

- ***However, Hashimoto fails to disclose, teach, or suggest a device wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.***

Maekawa - The arguments provided above regarding Maekawa are incorporated herein by reference.

Maekawa arguably discloses that in the first embodiment in FIG. 2, a source follower circuit has an NMOS source follower transistor 11 connected to a **power supply VCC** with the drain thereof and a current source 12 connected across the source of the source follower transistor 11 and earth (Maekawa at column 3, lines 23-27).

Maekawa arguably discloses that a current source 60 is connected across a **power supply VCC** and the common connection point of the gate of the cascode connected transistor 58 and the source follower transistor 59 (Maekawa at column 5, lines 51-54).

Maekawa arguably discloses that the gate potential of the cascode connected transistor 68 can be set to be higher than a **power supply voltage VCC** by the circuit operation accompanied by the on/off operation of the fourth analog switch 71 (Maekawa at column 7, lines 63-66).

- ***Nevertheless, the Office Action fails to show that Maekawa discloses a device wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.***

3. **The Examiner erred in rejecting claim 26 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).**

Claim 26 - Claim 26 is drawn to an electronic device capable of switching between a normal power consumption state and a low power consumption state, the electronic device comprising:

> the display device as claimed in claim 17, the matrix of pixels being within a display area; and
>
> a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode;
>
> wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

Hashimoto - The arguments provided above regarding Hashimoto are incorporated herein by reference.

Page 5 of the Office Action ***readily admits*** that Hashimoto fails to teach:

> a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode;
>
> wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

Ling - The Office Action cites Ling for the features that are deficient from within Hashimoto.

However, no timing diagram can be found within Ling.

- ***Thus, Ling fails to disclose, teach, or suggest a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Moreover, Ling arguably discloses that during the IDLE cycle, the R2R DAC 130 input is set to zero so that it consumes zero current, and the capacitor is fully charged to VREF voltage (Ling at column 3, lines 23-25).

Nevertheless, Ling ***fails*** to disclose, teach, or suggest driving of the display area being prohibited in the standby mode.

- ***Thus, Ling fails to disclose, teach, or suggest a device wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.***

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: July 16, 2009

Respectfully submitted,

By _____
Christopher M. Tobin
Registration No.: 40,290
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorneys for Applicant

CLAIMS APPENDIX

1-16. (Canceled)

17. A display device comprising:

a matrix of pixels, a pixel of said matrix of pixels having an electro-optic material between a pixel electrode and a common electrode;

a common driver having an offset circuit, a common voltage generated by said common driver being applied to said common electrode,

wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.

18. The display device as claimed in claim 17, wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage.

19. The display device as claimed in claim 18, wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.

20. The display device as claimed in claim 19, wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.

21. The display device as claimed in claim 18, wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.

22. The display device as claimed in claim 21, wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.

23. The display device as claimed in claim 17, further comprising:

a vertical driver connected to gate lines of said matrix of pixels;

a horizontal driver connected to signal lines of said matrix of pixels, said horizontal driver writing a signal voltage to said pixel electrode according to display data.

24. The display device as claimed in claim 23, wherein said level of said common voltage is adjusted with respect to said signal voltage.

25. The display device as claimed in claim 23, wherein said pixel of said matrix of pixels is located at an intersection of one of the gate lines and one of the signal lines.

26. An electronic device capable of switching between a normal power consumption state and a low power consumption state, the electronic device comprising:

the display device as claimed in claim 17, the matrix of pixels being within a display area; and

a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode;

wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.